Patent claims

1. Method for synchronization of external events which are routed to a component (CPU) and influence said component, in accordance with which the external events are buffered, with the stored external events being retrieved in a separate operating mode of the component for processing by an Execution Unit (EU) of the component and with the component in this operating mode responding to the fulfillment of conditions specifiable or predetermined by commands.

2. Method according to Claim 1,
characterized in that,
In accordance with an advantageous further development the specifiable condition is implemented by the change into the separate operating mode being executed, if a comparator element (K) of the component establishes a match between the instruction counter (CIC) and a register element (MIR) , with the content of the register element (MIR) being able to be specified by instructions and the counter (CIC) containing the number of instructions executed by the execution unit since the last change to the separate operating mode.

3. Method in accordance with one of the Claims 1 or 2,
characterized in that,
in redundant systems which feature at least two processor components (CPU) and in which an identical sequence of instructions is provided for the processor components (CPU) and identical external events can be retrieved by the components in the separate operating mode.

4. Method according to Claim 3,
characterized in that,
a faster component (CPU) is left in the separate operating

mode by a controller until a slower component has reached the end of the separate operating mode.

5. Processor component (CPU), with at least the following features:

- At least one Execution Unit (EU),
- At least one instruction counter element CIC for counting the instructions executed by the execution unit since the last change to the separate operating mode,
- At least one register element MIR for which the contents can be specified by instructions or is predetermined,
- At least one comparator element K to switch over the execution unit EU into a separate operating mode responding to the correspondence of the counter element CIC with the register element of MIR, with external events cached in the separate operating mode to be routed to the processor component (CPU) which influence the processor component (CPU) being retrieved by the processor component (CPU).

6. System consisting of at least two processor components (CPU), each with the following features:

- At least one Execution Unit (EU),
- At least one instruction counter element CIC for counting the instructions executed by the execution unit since the last change to the separate operating mode,
- At least one register element MIR for which the contents can be specified by instructions or is predetermined,
- At least one comparator element K to switch over the execution unit EU into a separate operating mode responding to the correspondence of the counter element CIC with the register element of MIR, with external events cached in the separate operating mode to be routed to the processor components which influence the processor components being retrieved by the processor components.

7. System in accordance with Claim 6, additionally featuring a connection between at least two of the processor components (CPU) which execute an identical instruction sequence, with the connection being provided for the transmission of synchronization information of the separate operating modes.